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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,858	06/02/2004	Masahiro SUNOHARA	031287a	3857

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ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP
1725 K STREET, NW
SUITE 1000
WASHINGTON, DC 20006

EXAMINER	
STARK, JARRETT J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,858	SUNOHARA ET AL.	
	Examiner	Art Unit	
	Jarrett J. Stark	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *12/05/2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1,2,3 is rejected under 35 U.S.C. 102(e) as being anticipated by Umetsu (US 2002/0127839A1).

Regarding claim 1, Umetsu shows in Figures 1 though 10 a method of manufacturing an electronic parts packaging structure, comprising the steps of:

flip-chip (1 shown in Fig 3) connecting a connection terminal of an electronic parts (10) having the connection terminal (90,140 shown in Fig. 3 & 8C) on an element forming surface to a wiring pattern(14, 16) formed on or over a base substrate;

forming an insulating film (22) in which the electronic parts are buried, on the electronic parts and the wiring substrate;

forming a via hole having a depth that reaches the connection terminal by etching a predetermined portion from an upper surface of the insulating film to the element forming surface of the electronic parts (24 shown in Fig 2A), and forming an overlying wiring pattern (14, 16), which is connected to the connection terminal via the via hole (24), on the insulating film(22).

Regarding Claim 2, Umetsu shows in Figures 1 though 10 a method of manufacturing an electronic parts packaging structure, comprising the steps of:

flip-chip (1 shown in Fig 3) connecting a connection terminal of an electronic parts (10), which has the connection terminal on an element forming surface and has a through electrode (40 shown in Fig 3) connected to the connection terminal via a first via hole (18 shown in Fig 1B) on a back surface, to a wiring pattern formed on or over a wiring substrate (14,16,40) shown in Fig 3);

forming an insulating film (22) in which the electronic parts are buried, on the electronic parts and the wiring substrate;

forming a second via hole (24 shown in Figure 2A) having a depth that reaches the through electrode, by etching a predetermined portion of the insulating film on the through electrode; and forming and overlying wiring pattern, which is connected to the through electrode via the second via hole, on the insulating film (Fig. 3).

Regarding Claim 3, Umetsu teaches in paragraph [0118] the method of manufacturing an electronic parts packaging structure, according to claim 1, wherein, in

the step of forming the via hole, the insulating film and the electronic parts are etched by RIE or a Laser.

Regarding claim 5, Umetsu teaches in Figure 1B → 2C, and paragraph [0128] a method of manufacturing an electronic parts package, according to claim 1, after the step of forming the via hole but before the step of forming the overlying wiring pattern (40 & paragraph [0128]), further comprising the steps of: forming an inorganic insulating film(22) on an inner surface of the via hole(18) and on the insulating film; and removing the inorganic insulating film from a bottom portion of the via hole to expose the connection terminal on the bottom portion of the via hole(Fig. 2A).

Regarding claim 6, Umetsu shows in Figure 4 a method of manufacturing an electronic parts packaging structure, according to claim 1, wherein a structure in which a plurality of electronic parts are stacked three-dimensionally in a multi-layered fashion and are connected mutually via the via hole is formed by repeating n times (n in an integer of 1 or more) respective parts to the wiring pattern to the step of forming the overlying wiring pattern.

Regarding claim 7, Umetsu shows in Figure 10 a method of manufacturing an electronic parts packaging structure, according to claim 1, after the step of forming the overlying wiring pattern, further comprising the step of: flip-chip connection a connecting terminal of an overlying electronic parts having the connection terminal to the overlying wiring pattern.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Umetsu (US Patent Application Publication 2002/0127839A1) in view of Furukawa (US Patent 6,365,513)

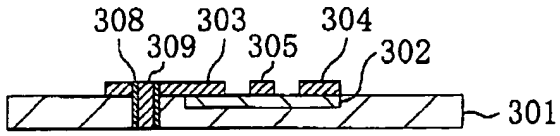
Umetsu teaches a method of manufacturing an electronic parts packaging structure, according to claim 1, wherein the step of forming the overlying wiring pattern includes the steps of, forming a resist film having an opening portion in a predetermined portion containing the via hole on the insulating film, forming a conductive film pattern in the via hole and the opening portion of the resist film.

Umetsu does not teach the formation of the conductive pattern in the via hole by applying a plating upward from the connection terminal exposed from a bottom portion of the via hole by means of electroplating that utilizes the wiring pattern and the connection terminal of the electronic parts connected to the wiring pattern as a planting power-supply layer.

Furukawa however discloses in Figure 3(e) and in columns 1-2 lines 62-6, this method of forming of the conductive pattern in the via hole by applying a plating

upward from the connection terminal (309) exposed from a bottom portion of the via hole by means of electroplating that utilizes the wiring pattern and the connection terminal of the electronic parts connected to the wiring pattern as a planting power-

Fig. 3(e)



supply layer (308).

Therefore, it would have been obvious to one of ordinary skill in the art to use a electroplating method to form the connection terminal. The option of electroplating as disclosed by Furukawa or the use of a laser to melt and form the connection terminal as shown by Umetsu is "merely a matter of obvious engineering choice".

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Umetsu (US Patent Application Publication 2002/0127839A1).

Regarding claim 8, a method of manufacturing an electronic parts package structure, according to claim 1, wherein the electronic parts is a semiconductor chip whose thickness is about 150 micrometers or less. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one of ordinary skill in the art to use a semiconductor chip whose thickness is about 150 micrometers or less. The thickness is "merely a matter of obvious engineering choice" as set forth in the above case law.

Response to Arguments

Applicant's arguments filed 12/05/2005 have been fully considered but they are not persuasive.

In regards to the argument that items 14 & 16 are "merely conductive pads and metal layers provided on the pads to prevent oxidation of the pads." The examiner directs the applicant to Umetsu, lines 2-3 of paragraph [116], "Each pad 14 is an electrode of an integrated circuit formed in the semiconductor chip 10." lines 13-15 of paragraph [116], also state "Note that a passivation film (not shown) may further be formed on the surface of the semiconductor chip 10 on which the pads 14 are formed."

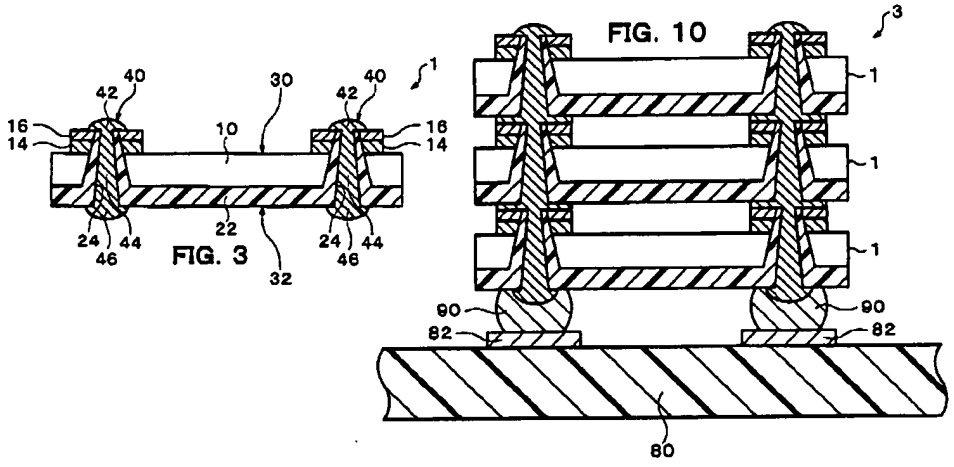


FIG. 3

Therefore there is an integrated circuit / wiring pattern formed on and/or in chip 10 and optionally covered by a passive / "insulating" layer (not shown in drawings) on one side and insulating film 22 on the other side. The package structure can be then mounted on a wiring substrate 80 as shown in figure 10.

Applicant's arguments with respect to claim 1 & 2 have been considered but are moot.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jarrett J. Stark whose telephone number is (571) 272-6005. The examiner can normally be reached on Monday - Thursday 7:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJS
December 13, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER